IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant :	Arun Ramakrishnan et al.	Appeal No. _____
Serial No.:	10/720,958	
Filed :	November 24, 2003	Group Art Unit: 2814
For :	ROUTING SCHEME FOR DIFFERENTIAL PAIRS IN FLIP CHIP SUBSTRATES	Examiner: Shrinivas H. Rao
Docket No.:	03-1098/L13.12-0252	

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION - 37 C.F.R. §41.37)

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12 DAY OF September, 20 05

David D. Brush
PATENT ATTORNEY

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on July 13, 2005.

FEE FOR FILING APPEAL BRIEF

Pursuant to 37 C.F.R. §41.20(b)(2) the fee for filing the Appeal Brief is $500.00.

The Director is authorized to charge any additional fees associated with this paper or credit any overpayment to Deposit Account No. 12-2252. A duplicate copy of this communication is enclosed.

Respectfully submitted,

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BRIEF FOR APPELLANT

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I HEREBY CERTIFY THAT THIS PAPER IS BEING SENT BY U.S. MAIL, FIRST CLASS, TO THE COMMISSIONER OF PATENTS AND TRADEMARKS, WASHINGTON, D.C. 20231, THIS

12 DAY OF September, 2005

Dan D. Bram

PATENT ATTORNEY

Sir:

This is an appeal from a final rejection of the claims in an Office Action dated April 20, 2005.

REAL PARTY IN INTEREST

LSI Logic Corporation, a corporation organized under the laws of the State of Delaware, and having offices at 1621 Barber Lane, MS D-106, Milpitas, California 95035, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefore, as set forth in the Assignment filed with the Patent Application and recorded on Reel 014747/Frame 0004.

RELATED APPEALS AND INTERFERENCES

Applicants are aware of no related appeals or interferences.

STATUS OF THE CLAIMS

Claims 1-32 are pending in the application and stand rejected based on cited references.

STATUS OF AMENDMENTS

An amendment after a Final Rejection was filed May 24, 2005, which was not entered.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates substrates used in flip chip packages for mounting semiconductor dies to integrated circuit boards. A "flip chip" refers to an integrated circuit that includes a semiconductor die, which is bonded circuit-side down to a substrate that is, in turn, bonded to a motherboard. (Page 1, lines 4-13).

The claims on appeal relate to the routing of differential signal pairs through the substrate. The input-output (I/O) signals on an integrated circuit die can include single-ended signals and differential signal pairs. Differential signal pairs are routed through the substrate from a pair of adjacent bumps on one side of the substrate to a corresponding pair of adjacent solder balls on the other side of the substrate. The conductive traces through the substrate of each signal in a differential signal pair are ideally identical to one another in terms of the length of conductive segments, the number of vias and the layers on which the conductive segments are routed. However, this becomes difficult due to the number of I/O signals and the density of the bumps in a typical flip chip package. (Page 2, line 26 to page 3, line 18; page 9, lines 1-13).

A. **Flip Chip Structure**

FIG. 1 is an exploded, perspective view of a flip chip 10, which can be mounted to a motherboard 12. Flip chip 10 includes an integrated circuit die 14 and a substrate 16. Die 14 is mounted face side down to substrate 16 within die bonding area 22. Die bonding area 22 includes edges 23, 24, 25 and 26, which define a perimeter of the die bonding area. (Page 7, lines 2-13).

Substrate 16 includes a plurality of conductive layers, such as a top layer 30, a second layer 31, a third layer 32 and a bottom layer 33, which are fabricated on a core 34 and are electrically isolated from one another. The bottom layer 33 of

substrate 16 is mounted to motherboard 12. The conductive layers on substrate 16 carry "traces" of conductive segments for interconnecting signals on die 14 with motherboard 16. (Page 7, line 14 to page 8, line 2).

FIG. 2 is a cross-sectional view of flip chip 10 mounted to motherboard 12. The face side of die 14 includes a plurality of "bumps" 50 to facilitate electrical connections from the die to the top conductive layer 30 of substrate 16. These bumps are densely packed together onto the small die. Substrate 16 spreads-out these densely packed bumps to a much less dense spacing so that the I/O signals along with power and ground can be connected to motherboard 12. (Page 8, lines 4-18).

A plurality of solder balls 52 are attached to the bottom conductive layer 33 of substrate 16 to facilitate the electrical interconnections between substrate 16 and motherboard 12. Each bump 50 is electrically connected to a corresponding one of the solder balls 52 through substrate 16. (Page 8, lines 19-29).

B. **Routing Difficulties for Differential Signal Pairs**

FIG. 3 illustrates the difficulty in routing differential signal pairs along and through the substrate. FIG. 3 shows a plurality of circular contacts on top conductive layer 30 of substrate 16, along edge 23 of die bonding area 22. These contacts are electrically and physically connected to corresponding bumps 50 shown in FIG. 2 when integrated circuit die 14 is bonded to substrate 16. (Page 9, lines 14-23).

Die bonding area 22 includes an I/O region 100 along die edge 23 and a central, core region 101. I/O region 100 has a pattern of contacts arranged in repeating units (shown by dashed lines). In this embodiment, each unit has eight contacts, including six contacts 104-109 for I/O signals, one contact for an I/O-level power conductor ("VDDIO") and one contact for an I/O-level ground conductor ("VSSIO"). Differential signal pairs

are routed to adjacent signal contacts within each unit 102. For example, contacts 104 and 106 can correspond to a first differential signal pair 130, contacts 107 and 109 can correspond to a second differential signal pair 132, and contacts 105 and 108 can correspond to a third differential signal pair 134. (Page 9, line 24 to page 10, line 16).

Due to the dense spacing of the contacts, there is typically not enough area between the contacts to route all of the traces from each contact in a particular unit 102 directly from the contact toward the corresponding die edge 23, on top conductive layer 30. The traces 122-123 for the first signal pair 130 can be routed together along the top conductive layer 30. The traces for the second signal pair 132 can be routed together along bottom layer 33 (shown in FIG. 1). (Page 10, line 17 to page 11, line 17).

However, the traces for contacts 105 and 108 of the third differential signal pair 134 cannot be routed together within die bonding area 22. Trace 121 for contact 105 can be routed outwardly on the top conductive layer, whereas the trace for other contact 108 must be routed downwardly to a different conductive layer and then outwardly toward die edge 123. This creates a potential difference in the routing lengths and impedances between the signals in the pair. (Page 11, lines 18-25).

Since the traces of a differential signal pair are typically required to be routed along the same layer in the substrate, the trace for contact 108 is re-routed back up to top layer 30 (for example), external to bonding area 22, so it can be routed adjacent to trace 121 along top layer 30. (Page 11, line 25 to page 12, line 2).

C. **Lateral Offset to reduce Trace Length Differences**

FIG. 5 is a diagram illustrating an escape pattern according to an embodiment of the present invention, which

reduces the difference in lengths between the traces for contacts 105 and 108 of the differential signal pair (as compared to FIG. 4). In this figure, the small dots correspond to the contacts shown in FIG. 3, and the large dots correspond to vias. (Page 12, lines 21-25).

In this embodiment, the escape pattern is defined so that via 170, which is used for jogging the trace for contact 108 to a different layer, is laterally offset from contact 108 in a direction toward contact 105 and the nearest die edge 23, as shown by arrow 142. If the traces for both contacts 105 and 108 are routed radially outward from die bonding area 22 toward the nearest die edge 23, this lateral offset will reduce the trace length difference within the substrate for the differential signal pair. (Page 12, line 25 to page 13, line 6).

D. **Routing Along Different Layers**

FIG. 6 schematically illustrates a side, cross-sectional view of substrate 16 showing the re-routing of the signal trace from contact 108 to bottom layer 33 and back to top layer 30. (Page 13, line 7 to page 14, line 24).

FIG. 7 illustrates an alternative routing scheme, which further reduces the trace length difference within the substrate for a differential signal pair. Instead of routing trace 150 outwardly from the die bonding area along bottom layer 33, conductive segment 154 is moved to second layer 31, which is adjacent to top layer 30, and routed outwardly along second layer 31. This further limits the length and impedance differences between the traces of the differential signal pair. (Page 14, line 25 to page 15, line 14).

E. **Lateral Offset on Bottom Layer**

The length differences can also be limited by modifying the trace routing pattern near the solder balls along bottom layer 33. FIG. 8 schematically illustrates a trace routing pattern of the differential signal pair to a pair of adjacent,

corresponding solder balls (or contacts) 182 and 184 on bottom layer 33. The conductive segments, vias and contacts on the various layers of substrate 16 are superimposed on one another on FIG. 8. (Page 15, line 15 to page 16, line 27).

Since the same design rules are often applied when routing the various conductive segments in traces 121 and 150 and when positioning the corresponding vias, both vias 178 and 197 (between bottom layer 33 and third layer 32) are offset in the same direction e.g., downward in FIG. 8 from the center of their corresponding solder ball contacts 182 and 184. This contributes to the length differences between traces 121 and 150. (Page 16, line 28 to page 17, line 12).

FIG. 9 is a schematic diagram of an alternative routing scheme having a modified lateral offset on bottom layer 33. The locations of conductive segments 158, 159 and 160 and vias 176 and 178 have been moved such that via 178 and conductive segment 160 on bottom layer 33 are laterally offset from the center of contact 184 in a direction toward the corresponding contact 182 in the differential pair. This further reduces the length and impedance differences between traces 121 and 150. (Page 17, lines 13-28).

With the above-modifications shown in FIGS. 5, 7 and 9, the trace lengths of a differential signal pair through a flip chip substrate can be better matched with one another. (Page 18, lines 1-17).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Whether the drawings comply with 37 C.F.R. 1.121(d) and 1.84(c).

II. Whether claims 1-32 are novel in view of Hosomi U.S. Publ. No. 2003/0209807, now U.S. Patent No. 6,768,206 (hereinafter Hosomi) (Exhibit B).

ARGUMENT

I. THE DRAWINGS COMPLY WITH THE PTO RULES

A. **Use of Brackets**

The Advisory Action indicated the amendment filed May 24, 2005 would not be entered. However, the Examiner confirmed by telephone on September 12, 2005 that the amendment to FIG. 1 is entered and now complies with PTO rules.

B. **Identifying Indicia**

Although the Advisory Action indicated that the drawings would continue to be rejected due to the location of identifying indicia, the Examiner confirmed in the telephone conversation on September 12, 2005 that this rejection would be withdrawn. If this status is incorrect, Applicants request an opportunity to brief this issue.

II. THE REJECTION OF CLAIMS 1-32

Claims 1-32 rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Hosomi U.S. Publ. No. 2003/0209807, now U.S. Patent No. 6,768,206 (hereinafter Hosomi) (Exhibit B).

Claims 1, 13 and 22 are independent claims, which are addressed separately below.

As described below, the figures and paragraphs of Hosomi that are cited in the Office Action do not support the rejection. Little or no similarity can be found, and entire elements are completely missing.

A. **Independent Claim 1**

1. Claim limitations

Independent claim 1 is directed to a flip chip substrate having first and second contacts on a top layer (within a die bonding area) and third and fourth contacts on a bottom layer, which correspond to a differential signal pair.

First and second traces are routed between the first and second contacts on a top layer and the third and fourth contacts, respectively, on the bottom layer.

The second trace is routed out of the die bounding area on a different one of the layers than the first trace. The second trace comprises a via in the die bonding area extending from the top layer to another of the plurality of layers. This via is laterally offset from the second contact in a direction toward the first contact.

In Fig. 5 of the present application, for example, first and second contacts 105 and 108 on the top layer (within the die bonding area) correspond to a differential signal pair. Via 170 is connected to contact 108 and extends from the top layer to another of the plurality of layers. Via 170 is laterally offset from the second contact (108) in a direction toward the first contact (105).

2. Hosomi Patent

The Office Action directs Applicants' attention to Hosomi figures 8-10 and paragraphs [0002], [0006], [0015], [0031] and [0032].

Contrary to the statement in the Office Action, Hosomi para. [0002] lines 3-7 and bumps 16 do not refer to differential signal pairs. Regardless, bumps 16 are on the die, not the substrate. Homsomi discloses metallic pads 20 on the substrate, but not a routing pattern for pads corresponding to a differential signal pair.

Regarding Hosomi para. [0006], lines 1-4, simply state that, "Traces (not shown) electrically interconnect pads 20 or 28 on either top surface 24 or bottom surface 30 of the substrate 14 or to vias (not shown) . . .." However Hosomi provides no guidance as to how traces for a differential signal pair can or should be routed relative to one another through the substrate.

Regarding Hosomi Figure 8 and para. [0015], Hosomi does

not disclose "the second trace [of a differential signal pair] is routed out of the die bonding area on a different one of the layers than the first trace [of the differential signal pair]," or that the second trace (of such a pair) comprises "a via in the die bonding area extending from the top layer to another of the plurality of layers," as recited in claim 1 of the present application.

Figure 8 simply shows a signal trace 110 routed in the space between two vias 70. (See para. [0015], lines 1-3). Figure 8 of Hosomi shows none of the elements mentioned above and is completely unrelated to the invention recited in claim 1. Hosomi does not suggest that trace 110 is electrically connected to either one of the vias 70 or that the vias 70 are related to one another.

The figure and the corresponding paragraph certainly do not disclose a second trace of a differential signal pair being routed out of a die bonding area on a different one of the layers than a first trace of the signal pair.

With respect to figures 9 and 10 and paragraphs [0031] and [0032], these figures show vertical columns 114 of pads 116 located at lattice points 118. The pads 116 are electrically connected to vias 120 also located at the lattice points 118. The pads 116 that overlie the vias 120 are referred to as "pad-on-vias" and are indicated by three concentric circles 122. Pads 140 without underlying vias 120 are located at interstitial points 142.

The signal pads are indicated by reference numerals 46 whereas core power pads are indicated by reference numeral 54, I/O power pads are indicated by reference numeral 56 and ground pads are indicated by reference numeral 58. The pads 140 without underlying vias 120 correspond to power and ground pads. The power and ground pads cannot be interpreted as being pads of a differential signal pair.

Further, the pad-on-via routing scheme does not provide leeway for positioning the vias at a laterally offset location relative to the corresponding contact. In fact, Hosomi does not disclose such an offset. Thus, the statement in the Office Action that suggests Hosomi discloses a via of a second trace, which is laterally offset from the second contact in a direction toward the first contact is incorrect. Hosomi discloses no such offset and particularly no offset with respect to differential signal pairs and their corresponding contacts.

The Hosomi patent does not mention differential signal pairs. Hosomi therefore does not teach how such pairs can be routed relative to one another through a flip chip substrate.

Hosomi does not disclose a second trace of a differential signal pair being routed out of a die bonding area on a different one of the layers than the first trace of the differential signal pair. Further, Hosomi does not disclose that such a second trace has a via in the die bonding area, which is laterally offset from the second contact in a direction toward the first contact.

Since Hosomi does not disclose numerous elements within independent claim 1, Applicants respectfully request that the rejection of claim 1 and its dependent claims 2-12 under §102(e) be reversed.

In addition, dependent claims 2-12 add further elements that are not taught by Hosomi, particularly in the context of differential signal pairs. These claims are addressed separately below.

B. **Independent Claim 13**

With respect to independent claim 13, this claim requires the first trace of the differential signal pair to have a first segment extending outwardly from the first contact toward an edge of the die bonding area along the top layer.

As shown in the embodiments of FIGS. 6 and 7, for example, the second trace (e.g., trace 150) extends from the second contact to a second one of the layers (e.g., layer LA04 or layer LA02) within the die bonding area. The second trace extends outwardly from the die bonding area (e.g., 23) along the second layer, and returns to the top layer (e.g., 30) externally to the die bonding area. Hosomi does not disclose such a routing pattern for a differential signal pair.

Claim 13 further requires the first and second traces to extend along the top layer outside the die bonding area to respective vias and extend downwardly from the respective vias toward the third and fourth contacts, respectively. Again, Hosomi does not disclose such a routing pattern.

Applicants therefore respectfully request that the rejection of claim 13 and its dependent claims 14-21 under §102(e) be withdrawn. Dependent claims 14-21 also include numerous other elements that are neither taught nor suggested by Hosomi, some of which are addressed below.

C. **Independent Claim 22**

Independent claim 22 requires the pair of vias extending from the bottom layer to be laterally offset toward one another relative to centers of the third and fourth contacts (of the differential signal pair) on the bottom layer. One embodiment is shown in FIG. 9 of the present application, which has contacts 182 and 184 on the bottom layer.

In this embodiment, first and second traces 121 and 150 comprise a pair of respective vias 178 and 197 extending from the bottom layer to another of the plurality of layers, wherein the pair of respective vias are laterally offset toward one another relative to centers of the third and fourth contacts 182 and 184 (of a differential signal pair), respectively. Again, Hosomi does not disclose such an offset.

Applicants therefore respectfully request that the rejection of independent claim 22 and its dependent claims 23-32 under §102(e) be withdrawn. Again, these dependent claims recite further elements and limitations that are neither taught nor suggested by Hosomi et al.

Accordingly, all claims 1-32 are patentable over the Hosomi reference.

D. **Dependent Claims 2 and 24**

Claims 2 and 25 require the first trace to be routed outwardly from the first contact toward an edge of the die bonding area along the top layer.

The second trace is routed from the second contact to the different layer and outwardly toward the edge of the die bonding area along the different layer.

As discussed above with respect to claims 1 and 13, Hosomi does not disclose routing a first trace (of a differential signal pair) out of a die bonding area along a top layer and a second trace (of the pair) outwardly along a different layer.

E. **Dependent Claims 3, 15 and 25**

With respect to claims 3, 15 and 25, Hosomi does not disclose first and second traces (of a differential signal pair) routed toward a nearest edge of the die bonding area. Hosomi is silent as to this feature.

F. **Dependent Claims 4 and 26**

Claims 4 and 26, due to their dependencies on previous claims, require the second trace (of the pair) to be routed from the second contact to the bottom layer (different than the first trace) and outwardly toward the edge of the die bonding area along the bottom layer.

Hosomi does not disclose two traces of a differential pair routed outwardly from a die bonding area on different layers, where the second trace is routed along a bottom layer.

G. **Dependent Claims 5 and 27**

Claims 5 and 27 require the second trace (of the pair) to be routed from the second contact to a different layer disposed between the top layer and the bottom layer and outwardly toward the edge of the die bonding area along the different intermediate layer.

Hosomi does not disclose two traces of a differential pair routed outwardly from a die bonding area on different layers, where the second trace is routed along an intermediate layer.

H. **Dependent Claims 6, 16 and 28**

Claims 6, 16 and 28 require the different layer on which the second trace (of the pair) is routed to be immediately adjacent to the top layer.

Hosomi is silent on this feature as well for a differential pair.

I. **Dependent Claims 7 and 29**

In claims 7 and 29, the second trace is routed from the different layer back up to the top layer externally to the die bonding area. As described with reference to claim 13, this feature is not disclosed by Hosomi.

Claims 7 and 29 also require the first and second traces to extend along the top layer outside of the die bonding area to respective vias located externally to the die bonding area and are routed downwardly from the respective vias toward the third and fourth contacts, respectively.

Again, this feature is completely absent in Hosomi.

J. **Dependent Claims 8, 17 and 30**

These claims require the vias referred to in claims 7, 13 and 29 to be located in a region on the top layer that is generally vertical of the third and fourth contacts. In claim 17, the vias are adjacent to one another.

Hosomi does not disclose such a trace structure within the context of the base and intermediate claims.

K. **Dependent Claims 9, 18 and 31**

With respect to claims 9, 18 and 31, Hosomi does not disclose first and second contacts of a differential signal pair, which form a pair of adjacent signal contacts in a die bonding area, within the context of the base claims.

L. **Dependent Claims 10 and 19**

With respect to claims 10 and 19, Hosomi does not disclose third and fourth contacts of a differential signal pair, which form a pair of adjacent signal contacts on the bottom layer, external to the die bonding area, within the context of the base claims.

M. **Dependent Claims 11, 20 and 32**

With respect to claims 11, 20 and 32, Hosomi does not disclose a second contact (of a differential signal pair), which is located further from a nearest edge of the die bonding region than the first contact (of the pair), within the context of the base claims.

N. **Dependent Claim 12**

As discussed with respect to independent claims 22, Hosomi does not disclose first and second traces comprising respective vias extending from the bottom layer to another of the plurality of layers, wherein the respective vias are laterally offset toward one another relative to centers of the third and fourth contacts, respectively.

O. **Dependent Claim 14**

As described with reference to independent claim 1, Hosomi does not disclose a second trace (of a differential signal pair) comprising a via extending from the top layer to a second layer within the die bonding area, wherein the via is laterally offset from a center of the second contact in a direction toward the first contact.

P. **Dependent Claim 21**

As described with reference to independent claim 22,

Hosomi does not disclose a pair of respective vias (of a differential signal pair) extending from the bottom layer to another of the plurality of layers, wherein the pair of respective vias are laterally offset toward one another relative to centers of the third and fourth contacts, respectively.

Q. **Dependent Claim 23**

As described with reference to independent claims 1 and 14, Hosomi does not disclose a second trace (of a differential signal pair) routed out of the die bonding area on a different one of the layers than the first trace (of the pair) and comprising a via in the die bonding area extending from the top layer to another of the plurality of layers, and wherein the via is laterally offset from the second contact in a direction toward the first contact.

CONCLUSION

For the above-reasons, Applicants respectfully request that the Board reverse the Examiner and find that claims 1-32 are in condition for allowance.

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APPENDIX 1

CLAIMS ON APPEAL

1. (Original) A flip chip substrate comprising:

a plurality of conductive layers, including a top layer and a bottom layer;

a first plurality of contacts, including first and second contacts corresponding to a differential signal pair, which are arranged on the top layer within a die bonding area;

a second plurality of contacts, including third and fourth contacts corresponding to the differential signal pair, which are arranged on the bottom layer; and

first and second traces routed between the first and third contacts and between the second and fourth contacts, respectively, wherein the second trace is routed out of the die bonding area on a different one of the layers than the first trace and comprises a via in the die bonding area extending from the top layer to another of the plurality of layers, wherein the via is laterally offset from the second contact in a direction toward the first contact.

2. (Original) The flip chip substrate of claim 1 wherein:

the first trace is routed outwardly from the first contact toward an edge of the die bonding area along the top layer; and

the second trace is routed from the second contact to the different layer and outwardly toward the edge

of the die bonding area along the different layer.

3. (Original) The flip chip substrate of claim 2 wherein the edge of the die bonding area is a nearest edge of the die bonding area to the first and second contacts.

4. (Original) The flip chip substrate of claim 2 wherein the different layer comprises the bottom layer, which is non-adjacent to the top layer.

5. (Original) The flip chip substrate of claim 2 wherein the different layer is disposed between the top layer and the bottom layer.

6. (Original) The flip chip substrate of claim 5 wherein the different layer is immediately adjacent to the top layer.

7. (Original) The flip chip substrate of claim 2 wherein:

the second trace is routed from the different layer back up to the top layer externally to the die bonding area; and

the first and second traces extend along the top layer outside of the die bonding area to respective vias located externally to the die bonding area and are routed downwardly from the respective vias toward the third and fourth contacts, respectively.

8. (Original) The flip chip substrate of claim 7 wherein the respective vias are located in a region on the top

layer that is generally vertical of the third and fourth contacts.

9. (Original) The flip chip substrate of claim 1 wherein the first and second contacts form a pair of adjacent signal contacts in the die bonding area.

10. (Original) The flip chip substrate of claim 1 wherein the third and fourth contacts form a pair of adjacent signal contacts on the bottom layer, external to the die bonding area.

11. (Original) The flip chip substrate of claim 1 wherein the second contact is located further from a nearest edge of the die bonding region than the first contact.

12. (Original) The flip chip substrate of claim 1 wherein:

the third and fourth contacts are adjacent to one another on the bottom layer; and

the first and second traces comprise respective vias extending from the bottom layer to another of the plurality of layers, wherein the respective vias are laterally offset toward one another relative to centers of the third and fourth contacts, respectively.

13. (Original) A flip chip substrate comprising:

a plurality of conductive layers, including a top layer and a bottom layer;

a first plurality of contacts, including first and second contacts corresponding to a differential signal pair, which are arranged on the top layer within a die bonding area;

a second plurality of contacts, including third and fourth contacts corresponding to the differential signal pair, which are arranged on the bottom layer;

a first trace electrically connecting the first and third contacts and having a first segment extending outwardly from the first contact toward an edge of the die bonding area along the top layer; and

a second trace electrically connecting the second and fourth contacts, wherein the second trace extends from the second contact to a second one of the layers within the die bonding area, which is located between the top and bottom layers, extends outwardly from the die bonding area along the second layer, and returns to the top layer externally to the die bonding area, and wherein the first and second traces extend along the top layer outside of the die bonding area to respective vias and extend downwardly from the respective vias toward the third and fourth contacts, respectively.

14. (Original) The flip chip substrate of claim 13 wherein the second trace comprises a further via extending from the top layer to the second layer within the die bonding area and wherein the further via is laterally offset from a center of the second contact in a direction toward the first contact.

15. (Original) The flip chip substrate of claim 13 wherein the first and second traces are routed outwardly along the top and second layers, respectively, toward a nearest edge of the die bonding area to the first and second contacts.

16. (Original) The flip chip substrate of claim 13 wherein the second layer is immediately adjacent to the top layer.

17. (Original) The flip chip substrate of claim 13 wherein the respective vias are located adjacent to one another in a region on the top layer that is generally vertical of the third and fourth contacts.

18. (Original) The flip chip substrate of claim 13 wherein the first and second contacts form a pair of adjacent signal contacts in the die bonding area.

19. (Original) The flip chip substrate of claim 13 wherein the third and fourth contacts form a pair of adjacent signal contacts on the bottom layer, external to the die bonding area.

20. (Original) The flip chip substrate of claim 13 wherein the second contact is located further from a nearest edge of the die bonding region than the first contact.

21. (Original) The flip chip substrate of claim 13 wherein:

the third and fourth contacts are adjacent to one another on the bottom layer; and

the first and second traces comprise a second pair of respective vias extending from the bottom layer to another of the plurality of layers, wherein the second pair of respective vias are laterally offset toward one another relative to centers of the third and fourth contacts, respectively.

22. (Original) A flip chip substrate comprising:

a plurality of conductive layers, including a top layer and a bottom layer;

a first plurality of contacts, including first and second contacts corresponding to a differential signal pair, which are arranged on the top layer within a die bonding area;

a second plurality of contacts, including third and fourth adjacent contacts corresponding to the differential signal pair, which are arranged on the bottom layer; and

first and second traces routed between the first and third contacts and between the second and fourth contacts, respectively, the first and second traces comprising a pair of respective vias extending from the bottom layer to another of the plurality of layers, wherein the pair of respective vias are laterally offset toward one another relative to centers of the third and fourth contacts, respectively.

23. (Original) The flip chip substrate of claim 22 wherein:

the second trace is routed out of the die bonding area on a different one of the layers than the first trace and comprises a via in the die bonding area extending from the top layer to another of the plurality of layers, and wherein the via is laterally offset from the second contact in a direction toward the first contact.

24. (Original) The flip chip substrate of claim 23 wherein:

the first trace is routed outwardly from the first contact toward an edge of the die bonding area along the top layer; and

the second trace is routed from the second contact to the different layer and outwardly toward the edge of the die bonding area along the different layer.

25. (Original) The flip chip substrate of claim 23 wherein the edge of the die bonding area is a nearest edge of the die bonding area to the first and second contacts.

26. (Original) The flip chip substrate of claim 23 wherein the different layer comprises the bottom layer, which is non-adjacent to the top layer.

27. (Original) The flip chip substrate of claim 23 wherein the different layer is disposed between the top layer and the bottom layer.

28. (Original) The flip chip substrate of claim 27 wherein the different layer is immediately adjacent to the top layer.

29. (Original) The flip chip substrate of claim 23 wherein:

the second trace is routed from the different layer back up to the top layer externally to the die bonding area; and

the first and second traces extend along the top layer outside of the die bonding area to a second pair of respective vias located externally to the die bonding area and are routed downwardly from the second pair of respective vias toward the first pair of respective vias, respectively.

30. (Original) The flip chip substrate of claim 29 wherein the second pair of respective vias are located in a region on the top layer that is generally vertical of the third and fourth contacts and the first pair of respective vias.

31. (Original) The flip chip substrate of claim 22 wherein the first and second contacts form a pair of adjacent signal contacts in the die bonding area.

32. (Original) The flip chip substrate of claim 22 wherein the second contact is located further from a nearest edge of the die bonding region than the first contact.

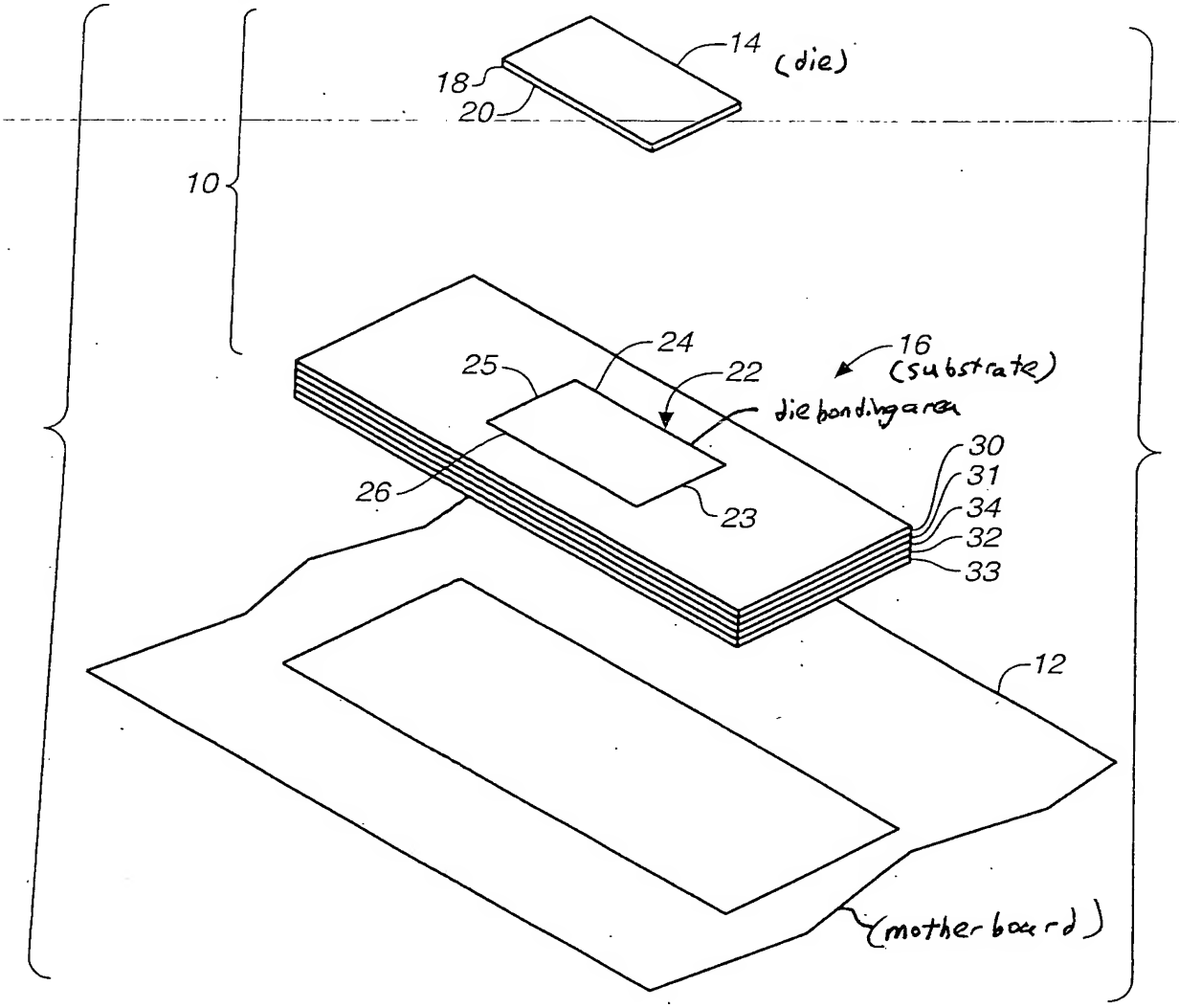

FIG._1

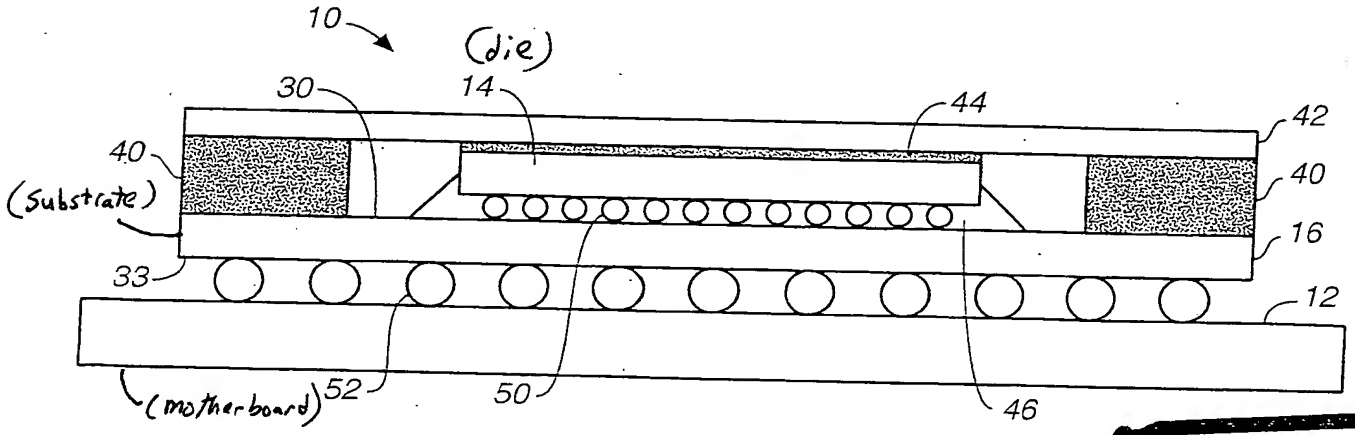

FIG._2

(top layer of substrate - contact pattern)

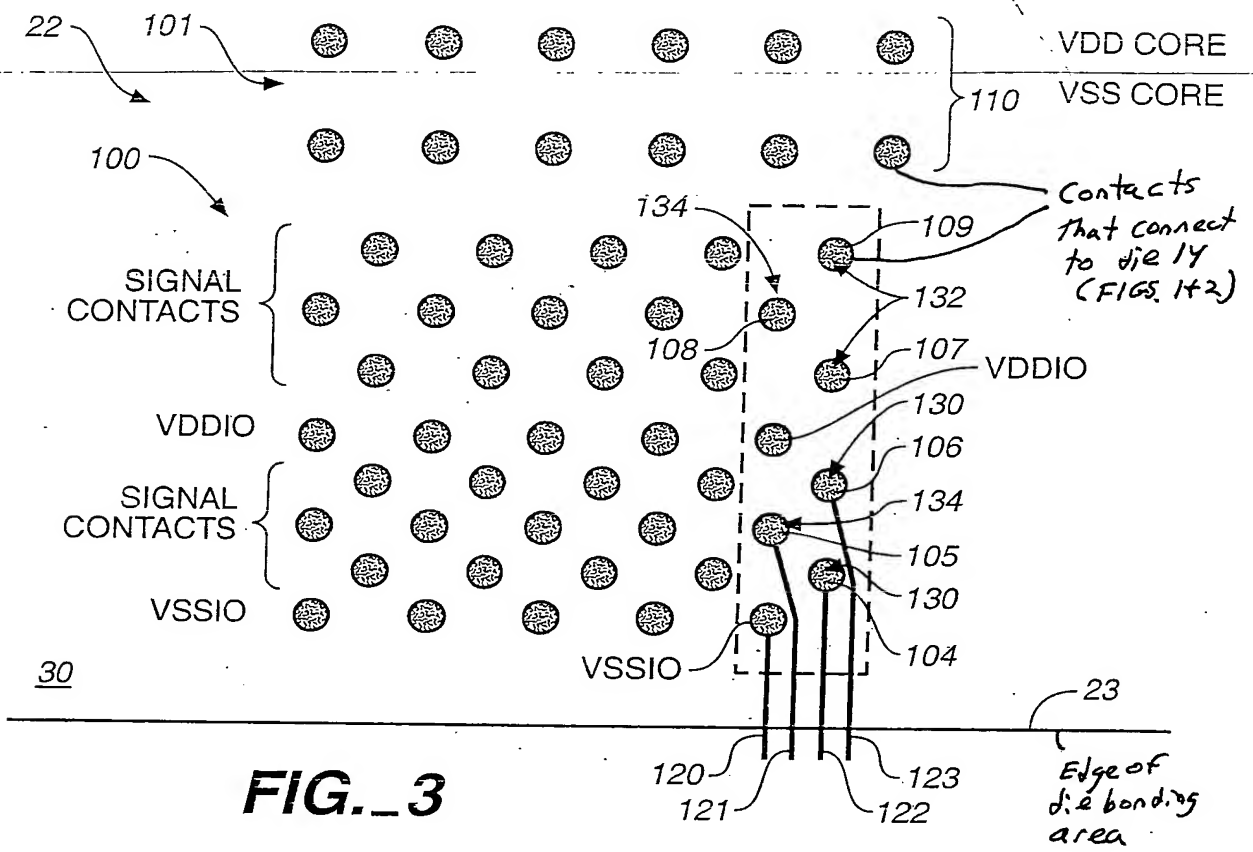

FIG._3

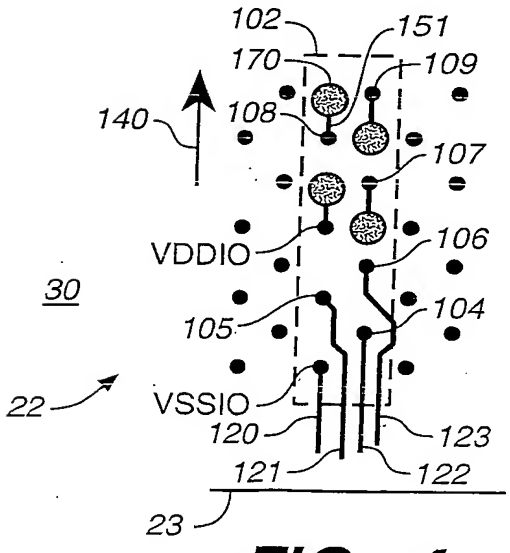

FIG._4

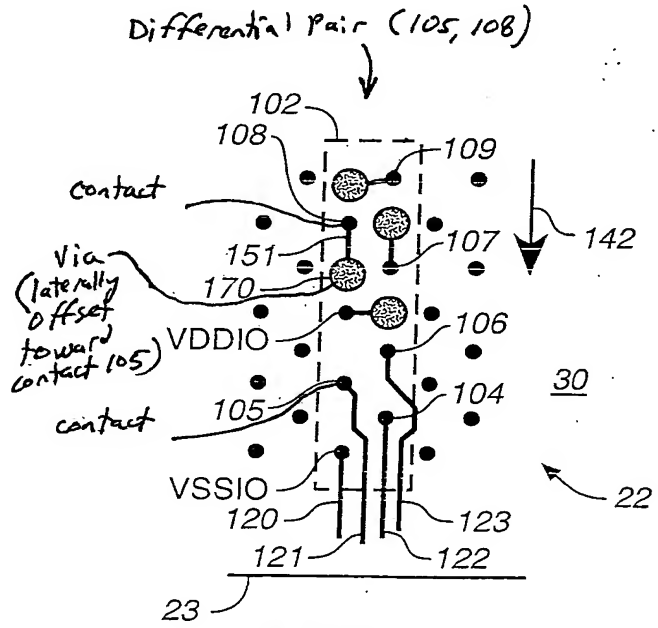

FIG._5

(Top layer)

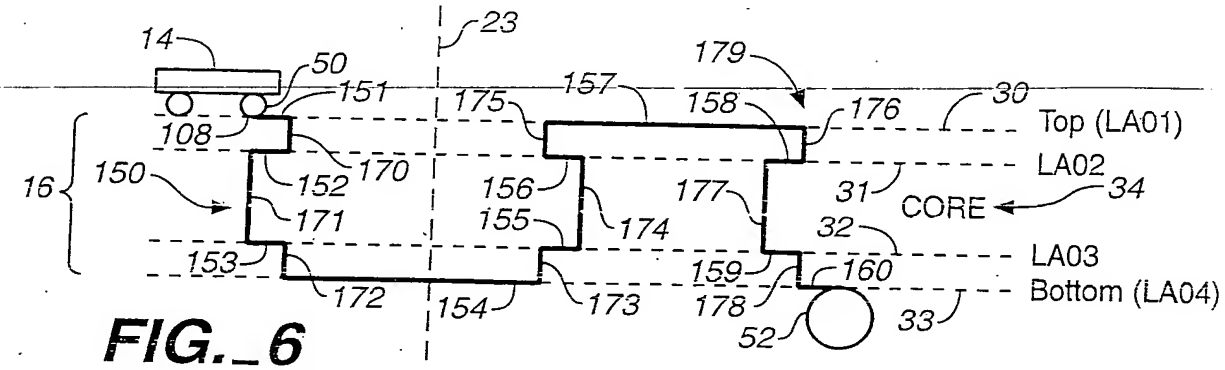

FIG._6

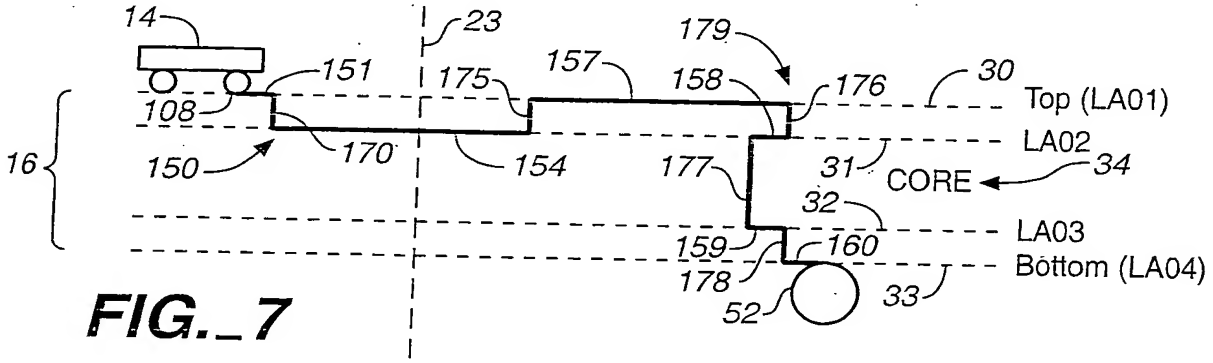

FIG._7

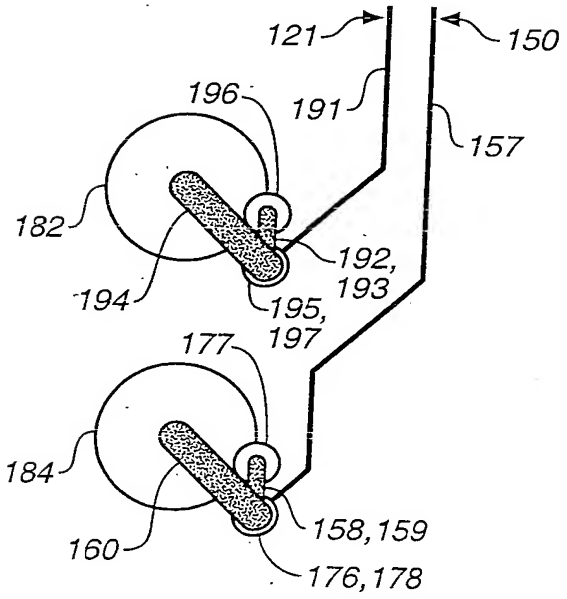

FIG._8

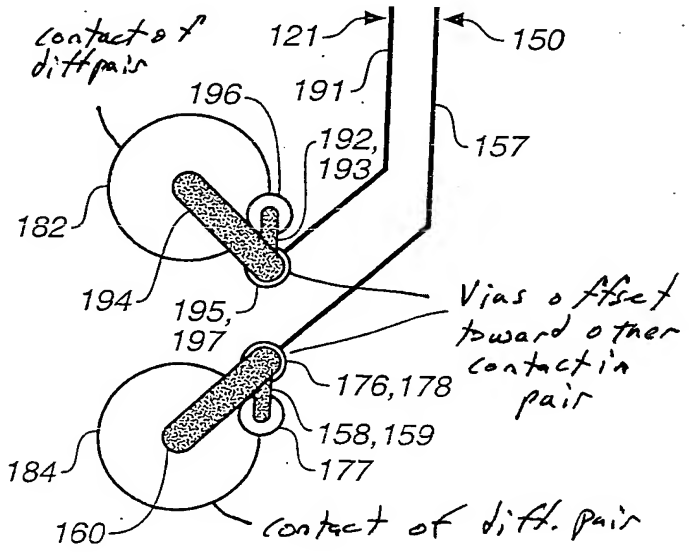

FIG._9

(contacts 182, 184 on Bottom layer)